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[MULTI-LEVEL MEMORY CELL AND FABRICATING METHOD THEREOF]

Abstract

A multi-level memory cell includes a substrate, an insulation layer, a silicon stripe, a first control gate, a second control gate, source/drain regions, silicon oxide/silicon nitride/silicon oxide composite layers. The insulation layer and the silicon stripe are sequentially disposed on the substrate. The first control gate and the second control gate are respectively disposed on the sidewalls of the silicon stripe, while the source/drain regions are configured in the silicon stripe beside both sides of the first control gate and the second control gate. The composite dielectric layers are disposed between the first control gate and the silicon stripe, and between the second control gate and the silicon stripe. Since a single memory structure can store a multiple bit of information, it is advantageous for minimizing devices.